

10035444-010402  
2040FO" 4445E00T

#### SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

BE IT KNOWN THAT WE, Fumikazu Yamaki, a citizen of Japan residing at Yamanashi, Japan and Takeshi Igarashi, a citizen of Japan residing at Yamanashi, Japan have invented certain new and useful improvements in

SEMICONDUCTOR DEVICE WITH A SUPER LATTICE BUFFER

of which the following is a specification : -

TITLE OF THE INVENTION

SEMICONDUCTOR DEVICE WITH A SUPER LATTICE BUFFER

CROSS-REFERENCE TO RELATED APPLICATION

5           The present application is based on Japanese  
priority application No.2001-003069 filed on January  
10, 2001, the entire contents of which are hereby  
incorporated by reference.

10   BACKGROUND OF THE INVENTION

          The present invention generally relates to  
semiconductor devices and more particularly to a high  
speed compound semiconductor device having a super  
lattice buffer.

15           In compound semiconductor devices, an active  
layer or a channel layer is formed by using a compound  
semiconductor, in which electron mobility is high, to  
attain high speed operation. Therefore, the compound  
semiconductor devices are important to high speed  
20 radio communication network systems employing GHz  
bands, including cellular phone service systems, and  
especially high power compound semiconductor devices  
are desired for base stations of such high speed radio  
communication networks.

25           FIG.1 shows the structure of a conventional  
MESFET 10 used as an output transistor at the final  
stage in a base station of a high-speed radio  
communication network system.

          Referring to FIG.1, the MESFET 10 is formed  
30 on a semi-insulating GaAs substrate 11, and includes  
an undoped GaAs buffer layer 12 formed epitaxially on  
the GaAs substrate 11, and an n-type GaAs channel  
layer 13 formed epitaxially on the buffer layer 12.  
On the channel layer 13 is formed a gate electrode 14G  
35 which corresponds to a channel region. A source  
electrode 14S and a drain electrode 14D are formed on  
opposite sides of the gate electrode 14G respectively,

1003544-010402

as shown in FIG.1.

FIG.2 is a chart illustrating the characteristic curves of drain-source currents  $I_{ds}$  versus drain-source voltages  $V_{ds}$  of the MESFET 10 of FIG.1. In this chart, a gate-source voltage  $V_{gs}$  is varied incrementally by 200mV each incremented to give many curves. The vertical axis represents the  $I_{ds}$  of the MESFET 10 with each division on the scale equalling 500mA, and the horizontal axis represents the drain-source voltage  $V_{ds}$  with each division of the scale equalling 2V.

Referring to FIG.2, the drain-source current  $I_{ds}$  increases as the gate-source voltage  $V_{gs}$  increases.

But after the  $I_{ds}$  reaches the saturation region, it suddenly drops as the drain-source voltage  $V_{ds}$  increases. It is known that this sudden drop of the saturated drain-source current  $I_{ds}$  is due to the Gunn Effect in the MESFET. As a result, the MESFET 10 has a limitation on high frequency power that can be obtained. The chart of FIG.2 shows the characteristic curves of the conventional MESFET 10 employing the semi-insulating GaAs substrate 11, and the substrate 11 has a high resistivity of more than  $1 \times 10^8$  Ohm-cm.

When high resistance semi-insulating GaAs is used as the substrate 11 shown in FIG.1 and a high voltage is applied to the channel layer 13, it will create multiple electric double regions comprising electron accumulation regions and electron depletion regions abutting on each other in turn. This is a domain structure and Gunn oscillation occurs.

FIG.3 is a schematic chart illustrating the characteristic curves shown in FIG.2 together with the load line of the MESFET 10.

Referring to FIG.3, the actual operational region of the MESFET 10 is located in the area where the saturated drain-source current  $I_{ds}$  suddenly drops.

204070-445007

Accordingly, the MESFET 10 cannot provide a desired high power output. In FIG.3, the minimum current of the saturated drain-source current  $I_{ds}$  in the Gunn oscillation area is represented by  $I_{dosc}$ . The minimum  
5 saturated drain-source current  $I_{dosc}$  is about 2400mA in the FIG.2 example.

Accordingly, conventional compound semiconductor devices cannot provide enough power when they are used for high power applications such as a  
10 base station output stage in high-speed radio communication systems. Various improvements in device structures have been tried in order to solve the above problems.

15 SUMMARY OF THE INVENTION

Accordingly, it is a general object of the present invention to provide a novel and useful semiconductor device wherein the foregoing problems are eliminated.

20 Another and more specific object of the present invention is to provide a high-speed semiconductor device that suppresses Gunn oscillation and can provide high power output.

Another object of the present invention is  
25 to provide a semiconductor device, comprising:

a compound semiconductor substrate having a resistivity less than  $1.0 \times 10^8$  Ohm-cm at least at surface thereof;

a buffer layer formed on the compound  
30 semiconductor substrate and having a super lattice structure; and

an active layer formed on the buffer layer and having an active element formed therein.

It is preferable to form the semiconductor  
35 device so that the compound semiconductor substrate has a resistivity less than  $0.6 \times 10^8$  Ohm-cm. Further, it is preferable to form the semiconductor device so

10035444-010402

that the active layer is formed at a position within 5.0  $\mu\text{m}$  of the surface of the compound semiconductor substrate. Further, it is preferable to have an electrode layer formed on another surface of the compound semiconductor substrate. Further, it is preferable to form the semiconductor device so that the electrode layer is not electrically connected to the semiconductor device. Further, it is preferable to form the semiconductor device so that the electrode layer is connected to one power supply potential of the semiconductor device. Further, it is preferable to have a source electrode and a drain electrode formed on the active layer separated from each other, so as to establish a channel region, and a gate electrode formed above the channel region. Further, it is preferable to form the semiconductor device so that the active layer has 2-Dimensional Electron Gasses. Further, it is preferable to form the semiconductor device so that the active layer comprises:

a collector layer of a first conducting type;

a base layer of a second conducting type formed on the collector layer;

an emitter layer of the first conducting type formed on the base layer. Further, it is preferable to form the semiconductor device so that the compound semiconductor substrate has a resistivity more than  $1.0 \times 10^8$  Ohm-cm in total. Further, it is preferable to form the semiconductor device so that the compound semiconductor substrate comprises a compound semiconductor support substrate having a resistivity more than  $1.0 \times 10^8$  Ohm-cm and a compound semiconductor having a resistivity less than  $1.0 \times 10^8$  Ohm-cm.

The inventors of the present invention have tried to inhibit large electrical fields from being

10035444-010402

10035444-010402

applied to the channel layer in the MESFET device 10 shown in FIG.1, in order to restrain the Gunn Effect. For that purpose, they have used a GaAs layer having a resistivity less than  $1.0 \times 10^8$  Ohm-cm as the

5 substrate 11 and tried to alleviate the concentration of electrical fields in the channel layer 13 along a depth direction. However, in this device having a combination of a high resistance GaAs buffer layer 12 and the low resistance GaAs substrate 11, the

10 electrical field concentration along the depth direction was truly alleviated in the channel layer 13, but electrons more easily accumulated around the interface between the buffer layer 12 and the substrate 11, as a result of the electrical field

15 alleviation, and therefore the domain became easier to generate. Because the interface between the buffer 12 and the substrate 11 is far from the gate electrode 14G or the drain electrode 14D, a horizontal electrical field, that is an electrical field parallel

20 to the substrate surface, became smaller, and then the electron density became higher and domains became easier to generate. This means that an ordinary high resistance GaAs buffer layer 12 cannot effectively inhibit electrons from leaking from the channel layer

25 13 to the low resistance substrate 11.

The inventors of the present invention, based on the above experience, have thought out a concept that in a compound semiconductor device including a MESFET device formed on a compound

30 semiconductor substrate, a low resistance substrate can be employed as the compound semiconductor substrate, and a buffer layer having a super lattice structure can be interposed between the low resistance compound semiconductor substrate and an active layer

35 having an active element formed therein. They found that such a device eliminates or alleviates the negative characteristics in the horizontal direction

of the buffer layer and effectively inhibits the domain generation unlike a conventional GaAs bulk buffer layer.

In a semiconductor device according to the present invention, it becomes possible to alleviate the electrical field concentration in an active layer even when a large electrical voltage is applied to the semiconductor device, by employing a compound semiconductor substrate, which has a low resistivity at least at one surface thereof. Further, according to the present invention, a high resistance buffer layer having a super lattice structure is interposed between the active layer and the substrate. As a result, it becomes possible to inhibit the electrons from leaking from the active layer to the interface between the low resistance substrate and the buffer layer, and it becomes also possible to inhibit the leaking electrons from accumulating at the interface. Further, it becomes possible to effectively restrain the domain generation in the buffer layer even under high electrical field conditions, by having such a super lattice structure in the buffer layer.

Other objects and further features of the present invention will become apparent from the following detailed description when read in conjunction with the attached drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG.1 is a cross-sectional view showing the construction of a conventional MESFET device;

FIG.2 shows the characteristic curves of the MESFET device shown in FIG.1;

FIG.3 shows the characteristic curves together with the load line of the MESFET device shown in FIG.1;

FIG.4 is a cross-sectional view showing the construction of a MESFET device according to a first

204070-4445007

embodiment of the present invention;

FIG.5 shows the characteristic curves of the MESFET device shown in FIG.4;

FIG.6 shows the characteristic curves  
5 together with the load line of the MESFET device shown in FIG.4;

FIG.7 shows the relationships between the minimum saturated drain-source current and substrate resistivities of the MESFET shown in FIG.4;

10 FIG.8 is a cross-sectional view showing the construction of a crystal growth apparatus for growing a low resistance GaAs substrate;

FIG.9 is a cross-sectional view showing the construction of a MESFET device according to a second  
15 embodiment of the present invention;

FIG.10 shows an alternative embodiment similar to the MESFET shown in FIG.9;

FIG.11 shows another alternative embodiment similar to the MESFET shown in FIG.9;

20 FIG.12 is a cross-sectional view showing the construction of a MESFET device according to a third embodiment of the present invention;

FIG.13 shows an alternative embodiment similar to the MESFET shown in FIG.12;

25 FIG.14 is a cross-sectional view showing the construction of a HBT device according to a fourth embodiment of the present invention; and

FIG.15 is a cross-sectional view showing the construction of a MESFET device according to a fifth  
30 embodiment of the present invention.

#### DETAILED DESCRIPTION OF THE INVENTION

##### [FIRST EMBODIMENT]

FIG.4 shows the construction of a MESFET 20  
35 according to a first embodiment of the present invention. Referring to FIG.4, the MESFET 20 is formed on a GaAs substrate 21 having a resistivity of

204070-445007



1 x 10<sup>8</sup> Ohm-cm. On the GaAs substrate 21 is formed a buffer layer 22 having a GaAs/AlGaAs super lattice structure, in which undoped GaAs layers each with a carrier concentration less than 1 x 10<sup>15</sup> cm<sup>-3</sup> and  
5 undoped AlGaAs layers each with a carrier concentration less than 1 x 10<sup>16</sup> cm<sup>-3</sup> are laminated alternately with the total thickness being in the range 100nm - 1 μm. In the buffer layer 22, both GaAs layers and AlGaAs layers typically have a thickness of  
10 10 - 100nm, and are formed preferably by the MOVPE method or the MBE method. The AlGaAs layers may preferably have a composition parameter x in the range 0.18 - 0.28 where the composition is represented by Al<sub>x</sub>Ga<sub>1-x</sub>As.

15 Further, on the GaAs/AlGaAs super lattice buffer 22 is formed a channel layer or an active layer 23 doped with Si to a concentration of 1 x 10<sup>17</sup> cm<sup>-3</sup> and having a thickness of about 200nm, by using the MOVPE method or the MBE method.

20 A source electrode 24S and drain electrode 24D are formed on the channel layer 23 so as to be in ohmic contact with it. A gate electrode 24G is formed on a channel region of the channel layer 23 between the source electrode 24S and the drain electrode 24D  
25 so as to be in Schottky contact with the channel layer 23.

FIG.5 is a chart illustrating characteristic curves of drain-source currents I<sub>ds</sub> versus drain-source voltages V<sub>ds</sub> of the MESFET 20 of FIG.4. In  
30 this chart, a gate-source voltage V<sub>gs</sub> is varied by 200mV increments to give many curves. The vertical axis represents the I<sub>ds</sub> of the MESFET 20 with one division of the scale being 500mA, and the horizontal axis represents the drain-source voltage V<sub>ds</sub> with one  
35 division of the scale being 2V, like Fig.2.

Referring to FIG.5, the drain-source current I<sub>ds</sub> increases as the gate-source voltage V<sub>gs</sub> increases.

204070" 445E00T

But after the  $I_{ds}$  reaches the saturation region, it drops as the drain-source voltage  $V_{ds}$  increases. These drops of the saturated drain current  $I_{ds}$  are significantly alleviated compared with the current drops in the conventional device shown in FIGs.1 and 2.

As seen from FIG.6 illustrating the combination of the characteristic curves and the load line, the device can avoid the bad influence of the Gunn Effect.

As shown in FIG.5, the MESFET 20 of FIG.4 improves the minimum value  $I_{dosc}$  of the saturated drain-source current in the Gunn oscillation region, from 2400mA to 3400mA.

FIG.7 shows the minimum saturated drain-source current  $I_{dosc}$  of the MESFET 20 of FIG.4 while the resistivity of the GaAs substrate 21 is gradually varied. In the actual experiments done by the inventors, instead of varying the resistivity, a variety of GaAs substrates commercially available and having different resistivities were used to give the minimum saturated drain-source current  $I_{dosc}$ .

Referring FIG.7, the minimum saturated drain-source current  $I_{dosc}$  increases when the resistivity of the substrate 21 is less than  $1.0 \times 10^8$  Ohm-cm, and on the other hand the minimum saturated drain-source current  $I_{dosc}$  decreases when the resistivity of the substrate 21 is more than  $1.0 \times 10^8$  Ohm-cm. When the resistivity of the substrate 21 is much smaller, for example, less than  $0.6 \times 10^8$  Ohm-cm, the minimum saturated drain-source current  $I_{dosc}$  increases much more.

In this embodiment, it is preferable that the distance between the substrate 21 and the channel layer 23 be equal to or less than the distance between the gate electrode and drain electrode in the FET in order that the low resistance substrate 21 may effectively alleviate the electric field concentration. The distance between a gate electrode and a drain

204070" tthSE00T

electrode in general FET devices is about 5 micrometers. Because the electrical field concentration generally occurs over a length corresponding to the above distance between two electrodes, the alleviation of the electric field concentration cannot be obtained when the distance between a low resistance substrate and a channel layer is greater than 5 micrometers.

Generally, a GaAs substrate can be manufactured by a method of pulling up its crystal from a liquid phase, such as the LEC method. During the process, natural lattice defects such as EL2 form donor levels in the GaAs crystal, and carbons from a graphite heater in a crystal growth apparatus form acceptor levels in the GaAs crystal, which constitutes a substrate. These reversal levels are compensated for to give a semi-insulating GaAs substrate in the prior art.

On the other hand, unintentional doping of the GaAs substrate by carbon should be inhibited when manufacturing a GaAs substrate with a low resistivity according to the present invention.

FIG.8 shows a substrate growth apparatus used for manufacturing a GaAs substrate with a low resistivity by the LEC method.

Referring FIG.8, the substrate growth apparatus 100 has a crucible 102 containing molten GaAs 102A in a pressure chamber 101. In the crucible 102 is provided a lid 102B made of  $B_2O_3$  covering the surface of the molten GaAs 102A, in order to restrain the dissociation and vaporization of As.

A graphite heater 103 is mounted within the pressure chamber 101. The crucible 102 is supported in a holder 104A that is mounted on a rod 104 movable upward and downward. A correctly oriented seed crystal attached at the tip of a pulling-up rod 105 is partly immersed in the molten GaAs 102A. The pulling-

10035444-010402

up rod 105 is rotated and slowly pulled up, and a GaAs ingot 106 is grown following the seed crystal.

In this embodiment, a surface of the graphite heater 103 is covered with Boron Nitride film, which avoids the problem of vaporized carbon being introduced in the molten GaAs 102A and then in the ingot 106.

[SECOND EMBODIMENT]

FIG.9 shows the construction of a MESFET 30 according to a second embodiment of the present invention. Those parts corresponding to the parts described previously are designated by the same reference numerals and the description thereof will be omitted.

Referring to FIG.9, the MESFET 30 has an undoped GaAs buffer layer 22A formed on a low resistance GaAs substrate 21. A GaAs/AlGaAs super lattice structure 22 is formed on the undoped GaAs buffer layer 22A. Another undoped GaAs buffer layer 22B is formed on the super lattice structure 22. A channel layer or an active layer 23 is formed on the undoped GaAs buffer layer 22B.

Also in this structure, it is possible to inhibit electrons from leaking to the interface between the substrate 21 and the undoped GaAs buffer layer 22A by the GaAs/AlGaAs super lattice structure 22 being interposed between the substrate 21 and the channel layer 23. As a result, the domain generation and Gunn oscillation under high power conditions can be avoided, as in the MESFET 20 shown in FIG. 4.

FIG.10 shows the construction of a MESFET device 30A according to an alternative embodiment, which omits the GaAs buffer layer 22B in the MESFET 30 shown in FIG.9. In this embodiment, the channel layer 23 is formed directly on the GaAs/AlGaAs super lattice structure 22.

204070"44500T

The MESFET 30A can also avoid the problem of the domain generation and the Gunn oscillation under high power conditions, as in the MESFET 30 of FIG. 9, because the GaAs/AlGaAs super lattice structure 22 is interposed between the low resistance GaAs substrate 21 and the channel layer 23.

FIG.11 shows the construction of a MESFET device 30B according to a further alternative embodiment, which omits the undoped GaAs layer 22A shown in FIG.9, resulting in the GaAs/AlGaAs super lattice structure 22 being formed directly on the low resistance GaAs substrate 21.

The MESFET 30B can also avoid the problem of the domain generation and the Gunn oscillation under high power conditions, as in the MESFET 30 of FIG. 9, because the GaAs/AlGaAs super lattice structure 22 is interposed between the low resistance GaAs substrate 21 and the channel layer 23.

#### [THIRD EMBODIMENT]

FIG.12 shows the construction of a MESFET 30C according to a third embodiment of the present invention. Those parts corresponding to the parts described previously are designated by the same reference numerals and the description thereof will be omitted.

Referring FIG.12, the MESFET 30C has a construction similar to that of the MESFET 20 shown in FIG.4, but is different in that it has an electrode layer 25 metalized on the bottom surface of the low resistance GaAs substrate 21. The electrode layer 25 can be used as a grounding electrode or a heat sink. Alternatively, the MESFET 30C can be brazed to an external heat sink via the electrode layer 25.

This electrode layer 25 in ohmic contact with the bottom surface of the substrate 21 can also alleviate the electric field problem in the substrate

204070" 4445E001

21. In this embodiment, it is preferable that the thickness of the substrate 21 be equal to or less than 5 micrometers, which approximately equals the distance between the gate electrode 24G and the drain electrode 24D, so that the electrode layer 25 is close enough to the channel layer 23. A conductor which is in Schottky contact with the substrate 21 can be used instead of the ohmic electrode layer 25, as long as its potential barrier is low enough.

10           The electrode layer 25 is not electrically connected to the channel layer 23 in the embodiment shown in FIG.12. Alternatively, as shown in FIG.13, a contact hall 21C may be opened through the super lattice buffer layer 22 and the channel layer 23, and  
15           the electrode layer 25 may be electrically connected to the source electrode 24S via a conducting plug 25A formed in the contact hall 21C.

[FOURTH EMBODIMENT]

20           FIG.14 shows the construction of a HBT 40 according to a fourth embodiment of the present invention.

Referring FIG.14, the HBT 40 is formed on a low resistance GaAs substrate 41 having a resistivity less than  $1.0 \times 10^8$  Ohm-cm. The HBT 40 includes a  
25           GaAs/AlGaAs super lattice buffer 42 formed on the GaAs substrate 41. The super lattice buffer 42 is made by laminating undoped GaAs layers and undoped AlGaAs layers alternately. The HBT 40 further includes an  
30           n<sup>+</sup>-type GaAs collector contact layer 43 formed epitaxially on the super buffer layer 42, an n-type GaAs collector layer 44 having a first mesa structure and formed epitaxially on the collector contact layer 43, a p-type GaAs base layer 45 formed epitaxially on  
35           the collector layer 44, an n-type AlGaAs wide gap emitter layer 46 having a second mesa structure and formed epitaxially on the base layer 45, and an n<sup>+</sup>-

10035444-010402

type GaAs emitter contact layer 47 formed epitaxially on the emitter layer 46. An n-type ohmic collector electrode 48C is formed on the collector contact layer 43, and a p-type ohmic emitter electrode 48E is formed on the emitter layer 47.

The HBT 40 can also inhibit the Gunn oscillation under high power condition, because the GaAs/AlGaAs super lattice buffer layer 42 is interposed between the low resistance GaAs substrate 41 and the collector contact layer 43.

[FIFTH EMBODIMENT]

FIG.15 shows the construction of a MESFET 50 according to a fifth embodiment of the present invention. Those parts corresponding to the parts described previously are designated by the same reference numerals and the description thereof will be omitted.

Referring FIG.15, the MESFET 50 has a construction similar to that of the MESFET 30, but is different in that it includes an n<sup>-</sup>-type GaAs buffer layer 52 having a carrier concentration high enough to alleviate electrical fields, instead of a high resistance GaAs buffer 22A. In this embodiment, because the electric field is alleviated in the buffer layer 52, a high resistance GaAs substrate 51 having a resistivity more than  $1.0 \times 10^8$  Ohm-cm can be used instead of the low resistance GaAs substrate 21.

The MESFET 50 was also found to avoid the problem of the domain generation and the Gunn oscillation under high power conditions, because the GaAs/AlGaAs super lattice buffer layer 22 is interposed between the substrate 51 and the channel layer 23 and the n<sup>-</sup>-type GaAs buffer layer 52 is interposed between the buffer layer 22 and substrate 51.

In this embodiment, a carrier concentration

10035444-010402

required for the buffer layer 52 varies depending on the thickness of the layer 52. The carrier concentration is preferably more than  $1 \times 10^{16} \text{ cm}^{-3}$  when the buffer layer 52 has a thickness of 300nm, and preferably more than  $1 \times 10^{15} \text{ cm}^{-3}$  when the buffer layer has a thickness of 1 micrometer. If the buffer layer 52 is too thick in this embodiment shown in FIG.15, it causes a problem in that a leak current passing through the buffer layer 52 increases.

Therefore, the thickness of the buffer layer 52 is limited within the above range in order that the layer 52 is depleted during the operation of the MESFET 50.

Although the above explanations were made using MESFET and HBT devices, the present invention is not limited to specific compound semiconductor devices and can be applied to other types of semiconductor devices including HEMT.

Further, although the above explanations were made using compound semiconductor devices formed on a GaAs substrate, the present invention can be applied to other types of compound semiconductor substrates such as one including InP, and the super lattice buffer layer 22 and the GaAs/AlGaAs super lattice barrier layer can still be used.

Further, the present invention is not limited to the embodiments described heretofore but various variations and modifications may be made without departing from the scope of the invention.

In a semiconductor device according to the present invention as set forth above, it becomes possible to alleviate an electric field concentration problem in a channel layer of the device under high power operating conditions, by employing a compound semiconductor substrate having a low resistivity at least in a surface area. Further, by interposing a high resistance buffer layer having a super lattice structure between the channel layer and the substrate,

204070" HHHSEOT



it becomes possible to inhibit electron leakage from the channel layer to the interface between the substrate and the buffer layer and restrain the leaking electrons accumulating at the interface.

- 5 Further, it becomes possible to effectively restrain the domain generation in the buffer layer under high power electrical field conditions, by having such a super lattice structure in the buffer layer.

204070" 445E00T  
10035444-010402